Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example at paragraph 0020:

"Referring to Figure 1F, a second main etch step is then carried out where the polysilicon layer 18 is etched through a second thickness portion, for example in one embodiment **to endpoint detection of an underlying gate dielectric layer 16 to at least partially expose the underlying gate dielectric layer**. In the second main etch step, at least the RF bias power and preferably both the RF bias power and the RF source power are reduced compared to the first main etch step. For example, preferably an RF source power is supplied between about 100 and about 300 Watts and an RF bias power is supplied form about 0 to about 100 Watts. Optionally no (zero) bias power is used. The lower RF source power together with the lower RF bias power,

preferably supplied at a frequency of greater than about 1 MHz, reduces ion bombardment energy and reduces electrical charge imbalance buildup at the exposed portions of the polysilicon gates."

PREMATURE FINALITY

Applicants respectfully request withdrawal of Finality since the newly applied art (Nallan et al.) was not necessitated by Applicants amendments, but rather, Applicants successfully disqualified formally applied Pan et al. Pan et al. (US 6,656,832) as a commonly owned reference. Since Applicants are entitled to a complete search and examination of their invention including reasonably anticipated limitations that may be claimed or disqualification of commonly owned references to avoid multiple searches resulting in piecemeal examination, Applicants respectfully request withdrawal of finality of rejection to either allow entry of the present amendments to place the application in condition for allowance or for an opportunity to meaningfully amend Applicants claims to define over the newly cited art.

For example, Applicants respectfully refer Examiner to the

following portions of the MPEP:

MPEP 706.07
Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied; and in reply to this action the applicant should amend with a view to avoiding all the grounds of rejection and objection. Switching from one subject matter to another in the claims presented by applicant in successive amendments, **or from one set of references to another by the examiner** in rejecting in successive actions claims of substantially the same subject matter, will alike tend to defeat attaining the goal of reaching a clearly defined issue for an early termination, i.e., either an allowance of the application or a final rejection.

MPEP 707.07(g) Piecemeal Examination
Piecemeal examination should be avoided as much as possible. The examiner ordinarily should reject each claim on all valid grounds available, avoiding, however, undue multiplication of references. (See MPEP § 904.03.)

MPEP 904.03
It is normally not enough that references be selected to meet only the terms of the claims alone, especially if only broad claims are presented; but the search should, insofar as possible, also cover all subject matter which the examiner reasonably anticipates might be incorporated into applicant's amendment. Applicants can facilitate a complete search by including, at the time of filing, claims varying from the broadest to which they believe they are entitled to the most detailed that they would be willing to accept.

MPEP 706.07(A)
Furthermore,a second or any subsequent action on the merits in any application or patent undergoing reexamination

> proceedings will not be made final if it includes a rejection, on newly cited art, other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17 (p), of any claim not amended by applicant or patent owner in spite of the fact that other claims may have been amended to require newly cited art. A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings **should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed**. See MPEP § 904 *et seq.*

Applicants therefore respectfully request withdrawal of finality.

Claim Rejections under 35 USC 103

1. Claims 1, 2, 4-9, 11-12, 14-19, and 21-22 stand rejected under 35 USC 103(a) as being unpatentable over Lee (5,665,203) in view of Nallan et al. (US 6,902,681).

Lee discloses a method for reactive ion etching of a gate electrode using an oxide hardmask layer and a three step silicon etching process. Lee discloses disclose etching with CF4 **in a first chamber** to remove any oxide that may have formed on the polysilicon layer during stripping of the resist mask (col 4,

lines 31-35). After transfer to a silicon etching chamber a second step is carried out using **HBR/CL2/O2** in a first silicon etching step (second etching step)(col4, lines 34-36) and then **HBR/O2** in a third etching step(second silicon etching step)(col 4, lines 52-67).

Lee overcomes the problem of etching polysilicon gates **to obtain vertical sidewalls (see col 1, lines 5-9) by oxidizing the sidewalls of the silicon during the first silicon etch step** (second etch step) (col 1, lines 63-66; col 4, lines 38-46) and **stopping a predetermined distance (20 nm) above the gate oxide layer (without exposing the gate oxide), then** removing substantially all CL2 from the etching chamber atmosphere (col 2, lines 1-5; col 4, lines 47-51), and **then etching through a remaining thickness portion of the silicon layer to expose the gate oxide layer** (col 2, lines 1-5; col 4, lines 52-64) **where the second silicon etch step (third etch step) includes an overetch process**. Lee discloses using low pressure and low power density in the second silicon etch step to expose the gate oxide layer with **no magnetic field enhancement** (col 4, lines 64- col 5, line 3). Lee discloses "a fourth step in the gate etch process" of **dipping in HF to remove oxide residues** from the gate sidewalls (col 5, lines 4-6).

Applicants respectfully point out that Examiner has misinterpreted Lee by asserting that the overetch time included in the "**third step" of the gate etch process** taught by Lee at col 4, lines 52-64 is a fourth RIE etch step. Lee et al., clearly disclose and teach that the **overetch time** is **included** in the **third step of the gate etch process** which is "based on the time for the **final etch step to reach the gate oxide**" (col 4, lines 58-60).

More importantly, **Lee nowhere discloses or suggests performing a plasma treatment following endpoint detection and exposure of portions of an underlying gate dielectric.**

On the other hand, Nallan et al. disclose a method of etching high dielectric constant materials using a halogen gas, reducing gas, and passivating gas chemistry (see Abstract) to overcome the problem of oxidation of the polysilicon electrode to prevent degradation of the gate structure (col 1, lines 27-45). In one embodiment, the passivating gas (N2) is including in the etch gas of Cl2, CO, and N2 during etching of a high-K gate dielectric (to remove most or all of the gate dielectric to expose the silicon wafer) and in another embodiment the

passivating gas is used after etching to passivate the exposed silicon (col 1, lines 52-62; col 2, lines 51-65). The passivating gas N2 may be optionally mixed with one or several inert gases (col 2, lines 48-50).

Nallan et al. generally disclose that a polysilicon gate electrode has previously been etched (prior to etching the high-K gate dielectric) and is used as an etch mask in etching the high-K gate dielectric, **but do not disclose or teach a process for etching a gate electrode** (col 6, lines 34-49).

Nallan et al. generally disclose that **in the two step gate dielectric process;** (first etching through the high-K gate dielectric to expose the silicon wafer **and then treating with a passivating plasma using nitrogen** (and one or more inert gases) that the nitrogen plasma **forms nitride layers** on the exposed portions of the silicon (wafer) and polysilicon (gate electrode) as well as forming an HfON layer on hafnium oxide (high-K gate dielectric) (col 5, lines 40-56) which thereby inhibits oxidation during a subsequent post-etch oxygen plasma cleaning step.

There is no apparent motivation for combining the disparate teachings of Nallan et al., who **teach a gate dielectric etching**

process including a plasma treatment process including nitrogen to **form nitride layers** on **exposed silicon or polysilicon** following the gate dielectric etching process with the method of Lee who discloses a **gate electrode etching process** that **reaches the gate oxide in the final poly silicon-etch step which is then overetched in the same etch step.**

Moreover, modifying the process of Lee (who teaches a fourth HF dip etch to t=remove oxide residues on the polysilicon gate) by the process of Nallan, who teaches forming nitride layers in a nitrogen plasma treatment to protect the exposed silicon and polysilicon in a subsequent oxygen plasma cleaning process, would make the process of Lee unsuitable for its intended purpose (i.e., HF etch would not remove nitride layers and the process of Lee is inconsistent with an oxygen plasma cleaning process).

Even assuming *arguendo*, a proper motivation for combining the teachings of the gate dielectric etching process of Nallan et al. with the gate electrode etching process of Lee et al., such combination does not produce Applicants disclosed and claimed invention.

The combined references nowhere teach or suggest **Lee nowhere**

discloses or suggests performing Applicants inert gas plasma treatment following endpoint detection of an underlying gate dielectric (claim 1) or prior to a subsequent overetch process (claim 14).

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

2. Claims 3, 10, 13, 20, and 23 stand rejected over Lee and Nallan et al., above, and further in view of Lill et al. (US 6, 284,665).

Applicants reiterate the comments made above, with respect to Lee and Nallan et al.

Lee discloses the use of a **low bias voltage** in the range of 50 to 100 Volts to avoid ion damage to the gate oxide layer (col 2, lines 46-49) **in a polysilicon etchback (planarization etching) process with an underlying silicon nitride layer.**

The fact that Lill et al. teach typical process conditions for RIE etching of polysilicon selectively to silicon nitride **in a polysilicon etchback (flat etch front) process** including the use of a low bias Voltage or no bias Voltage, does not further help Examiner in establishing a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the disparate teachings of plasma process conditions for a polysilicon etchback process (Lill et al.) with a high-K gate dielectric etching process (Nallan et al.) with a polysilicon gate electrode etch process (Lee) where an inert gas plasma treatment is neither suggested or disclosed as part of a gate electrode etching process, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

3. Claims 1-23 stand rejected over Schoenborn (US 5,242,536) in view of Lee et al. (US 5,665,203) and Kim et al. (US 6,620,575) and Winniczek et al (US 6,093,332) and Nallan et al. (6,902,681).

Applicants reiterate the comments made above with respect to Lee et al. and Nallan et al.

Examiner again relies on Nallan for the teaching of Applicants claimed inert gas plasma treatment where nitrogen and one or more inert gases are used in a plasma treatment **to form a protective nitride layer following etching of a gate dielectric to expose underlying silicon** as outlined above.

Examiner asserts that Schoenborn discloses a polysilicon etch process similar to Lee using minimal etching bias and low power **but is silent on RF source and bias power** in Applicants second etch step or a lower etch power or bias power in Applicants third step.

Examiner asserts that Kim et al teach a polysilicon etch with RF power at both source and bias and the bias power are adjustably decoupled from the source.

Examiner asserts that Winniczek teaches a **pulsed RF power** to the chuck which Examiner therefore asserts **includes zero RF power** to reduce polymer deposition on a mask. Applicants assert that one of ordinary skill would not interpret a pulsed RF power to be equivalent to Applicants claim language in light of the Specification "**wherein the step of plasma treating is carried out using zero RF bias power**" as in Applicants claim 2 and 14.

Even assuming *arguendo*, that the above references teach what the Examiner asserts, and assuming *arguendo* a motive for combination, such combination does not produce Applicants disclosed and claimed invention.

The combined teachings nowhere suggest or disclose Applicants claimed gate electrode etching process in combination with Applicants inert gas plasma treatment **including following endpoint detection of a gate dielectric underlying a polysilicon layer.**

Thus, the combination of the teachings of Nallan with the other cited references does not produce Applicants disclosed and claimed invention.

Moreover, none of the cited references, singly or in combination, recognize or provide a solution to the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in a polysilicon gate electrode etching process".

Moreover, none of the cited references suggest or disclose Applicants polysilicon gate electrode etch process in combination with Applicants inert gas plasma treatment "to neutralize an electrical charge imbalance".

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

"Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered." See, e.g., *Diamond v. Diehr*, 450 U.S. at 188-189, 209 USPQ at 9.

Examiner is required to interpret the claims by giving the terms thereof the broadest reasonable interpretation in their ordinary usage as they would be understood by one of ordinary skill in the art in light of the written specification, including drawings, unless another meaning is intended by appellants as established in the written specification, and without reading into the claims any limitation or particular embodiment disclosed

in the specification. *See e.g., In re Morris*, 127 F.3d. 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir 1997); *In re Zeltz* (893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Conclusion

The cited references, alone or in combination, fail to produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

Applicants have amended the claims to clarify their disclosed and claimed invention and respectfully request favorable reconsideration by Examiner.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his

Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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